Workshop on "Advanced Computer Architectures and Dependable Embedded Systems" by Tallinn University of Technology

Background

Innovative chip manufacturing technologies are the key enabling factors for modern IT systems. Driven by Moore's Law, the functional integration density on microchips permanently increasing. This enables hardware and system designers to successfully realize advanced System-on-Chip solutions for embedded computing (mobile phones, computing pads, photo cameras, medical devices, automotive electronics, avionic systems, infotainment products), which have strict demands for low power consumption at increasing functional complexity. In the field of high-performance computing similar requirements are becoming more and more important: scalable multiprocessor computing systems on different integration levels: Multi-Processor System-on-Chip (MPSOC), servers, data centers, private and public clouds.

Learning outcomes

In this workshop the participants will learn about systematic and CAD supported structuring of hardware and computer architectures. First we derive some basic methods for architectural synthesis. Then we will step up several layers of abstraction and analyze how this method can be used for the design of complex on-chip multiprocessor architectures. In this context advanced on-chip communication architectures are an integral part of this course.

The workshop will be held in two parts of total 6 academic hours

1. Introduction to CAD methods for Hardware and System Architecture Synthesis:
    a. Introduction to CAD methods for chip and system design
    b. Synthesis of processing architectures out of sequential program code (Architectural Synthesis
    c. Efficient resource usage by application of scheduling methods
2. Advanced On-Chip Multiprocessor Architectures with Network-on-Chip Communication
    a. Networks-on-Chip as efficient on-chip communication architectures: topologies, switching and routing methods
    b. Multiprocessor Systems-on-Chip (MPSoC) based on 3D chip stacking
    c. Virtualization and Dependability/Reliability concepts for MPSoCs

Target audience

Students in the 3rd and last year of their Bachelor study or in master studies in the fields of Computer Engineering, Electronics Engineering, Mechatronics, Computer Science. Students should have a good knowledge on logic circuit design and logic optimization and computer architectures (controllers, data-paths). Furthermore some know-how on hardware modeling and sequential an object-oriented programming will be helpful as well as some basic know-how on optimization methods and complexity theory.

Number of participants: **30 students** for optimal result. With instructor's consent, more students can be accepted.

Instructor: to be decided

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Special benefits for workshop participants

- Diploma upon completion of the workshop
- Application fee waive for those who apply for Tallinn Tech study programs: you save 50 euro* for bachelor and 100 euro for master,
- Discount of 250 euro for English Language Preparatory Year,
- Discount of 15% for the Summer School: you save 370 euro if register before 1st of May or 385 euro if register after 1st of May,
- Discount of 20% for European Innovation Academy (EIA): you save 90 euro if register one course, and 158 and 210 euro if register two and three courses respectively.

* 1 euro = ca 8,41 yuan (based on the Bank of China exchange rate on Feb 15, 2013)

More information

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